Advanced Packaging Technologies usher in a new era in the semiconductor marketplace

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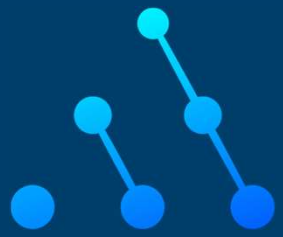


Semiconductor
Sector Service
Bureau

Take aways from this talk

- Advanced packaging technologies will re-enable widespread use of custom semiconductor designs in products worldwide
- S3B is influencing the positioning and growth of semiconductor activities in Australia
- Building and operating advanced packaging plants in Australia
  + Gaining access to semiconductor global supply chain companies
  will make us competitive in mainstream semiconductor and other markets

CAD Licenses

Training and Fundamental Research

High license costs and accessibility compared to Europe, North America and Taiwan

Major change for academic licenses following discussions with Cadence:

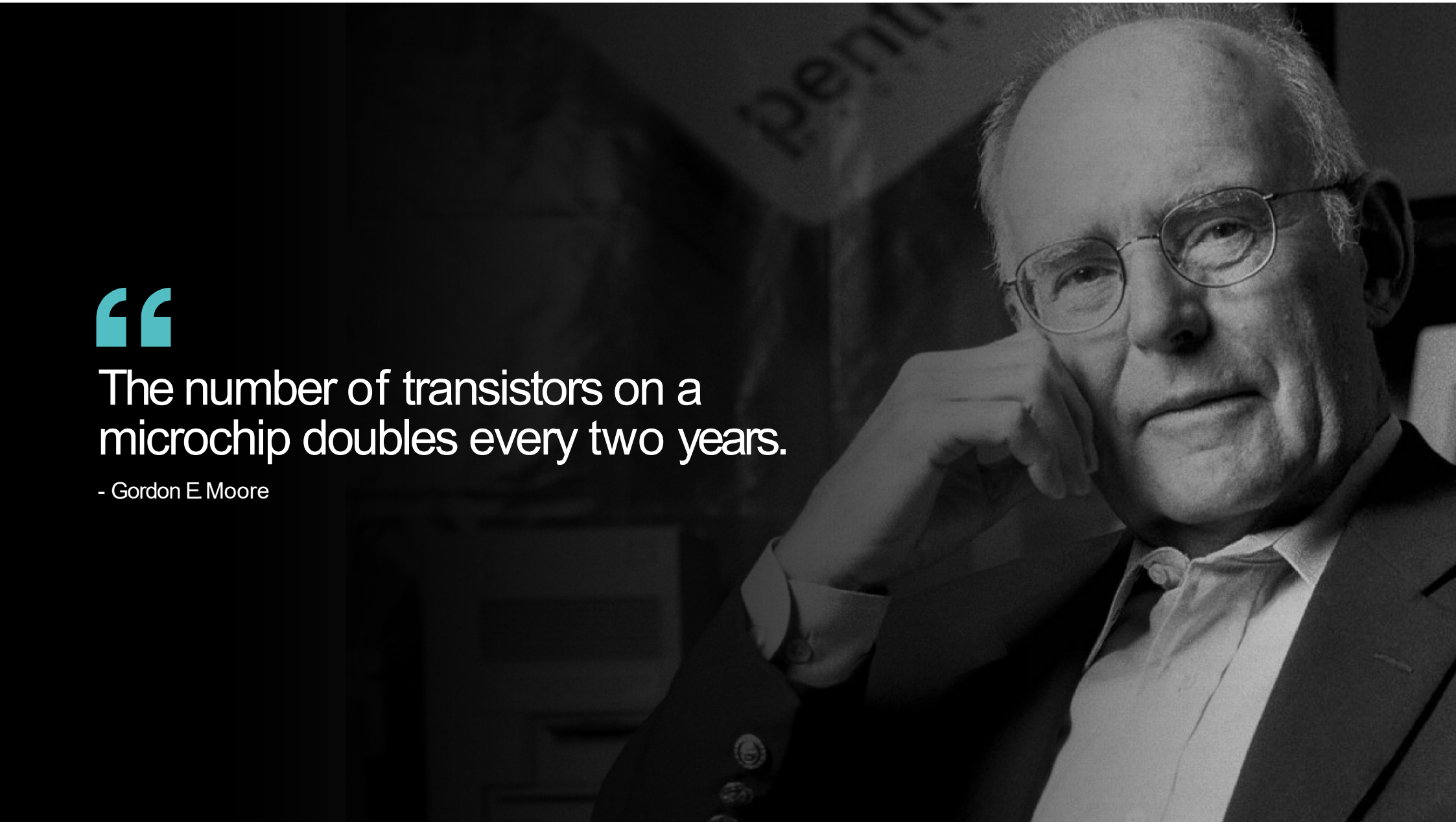
US Style university program rolled out across country
Substantial discounts for teaching and fundamental research purposes.

Start-ups

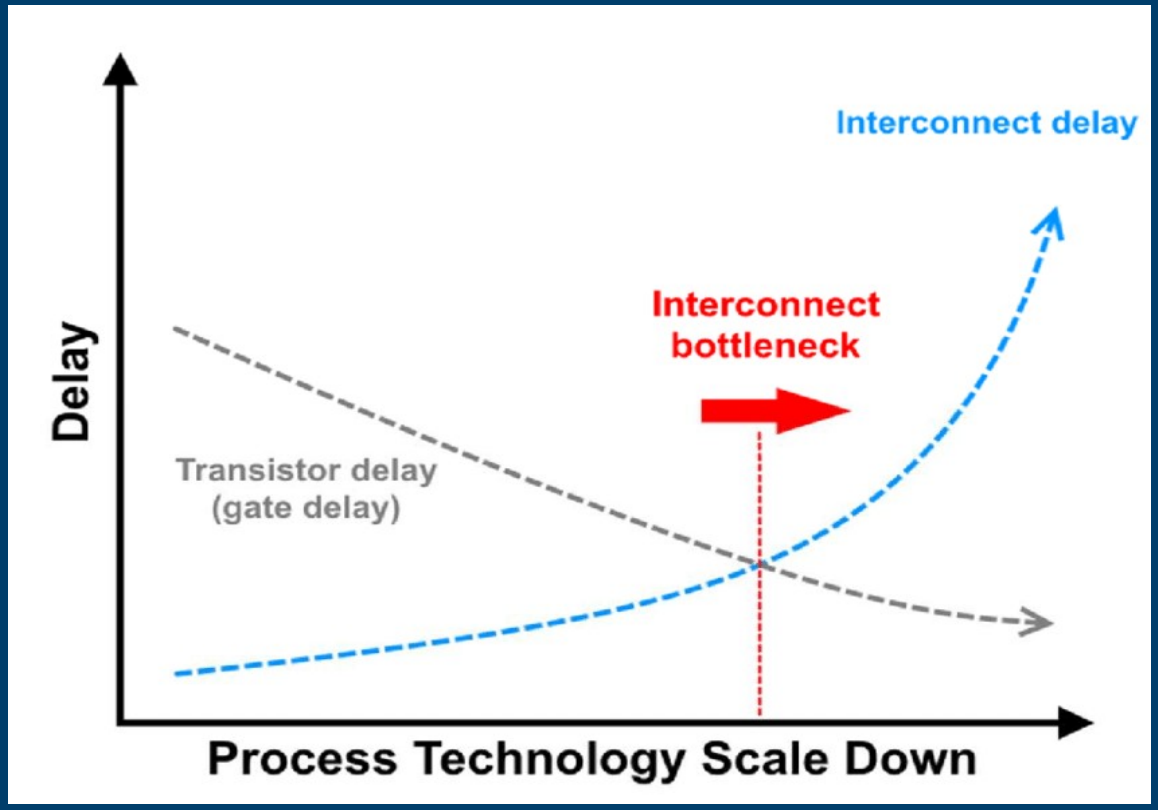
Facilitated introductions between start ups and vendors

Begun discussions with CAD vendors around start-up programs

Idea is to host a pool of licenses accessible to start-ups – promising discussions ongoing

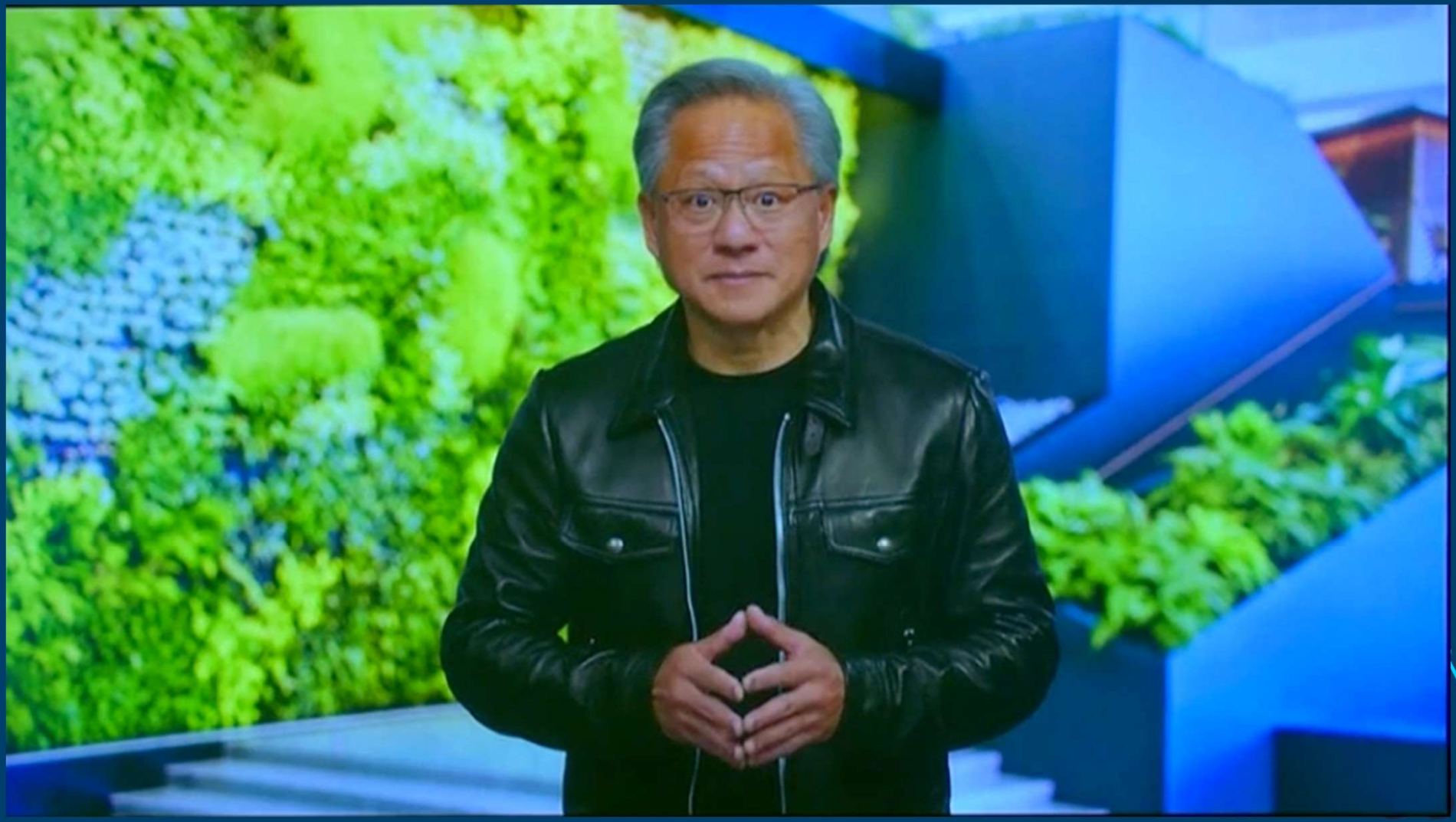

“
The number of transistors on a microchip doubles every two years.
- Gordon E. Moore

Effective End of Moore's Law - Its All About The Wire

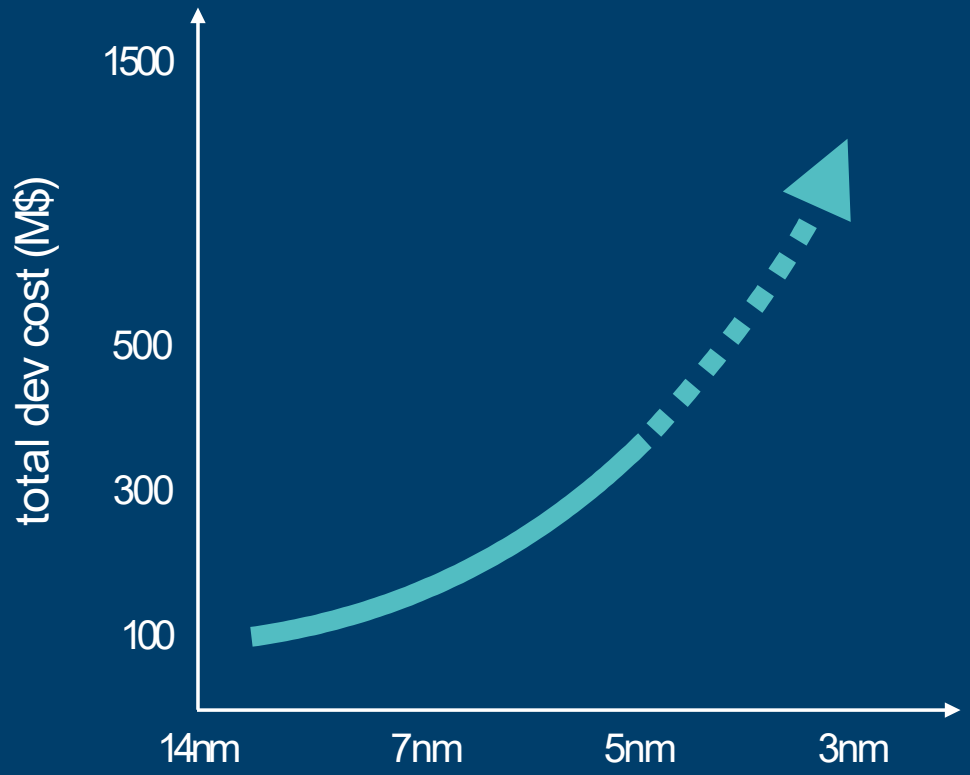


Source: NHANCED SEMICONDUCTORS

3nm Lithography – Jensen Huang – Nvidia CEO

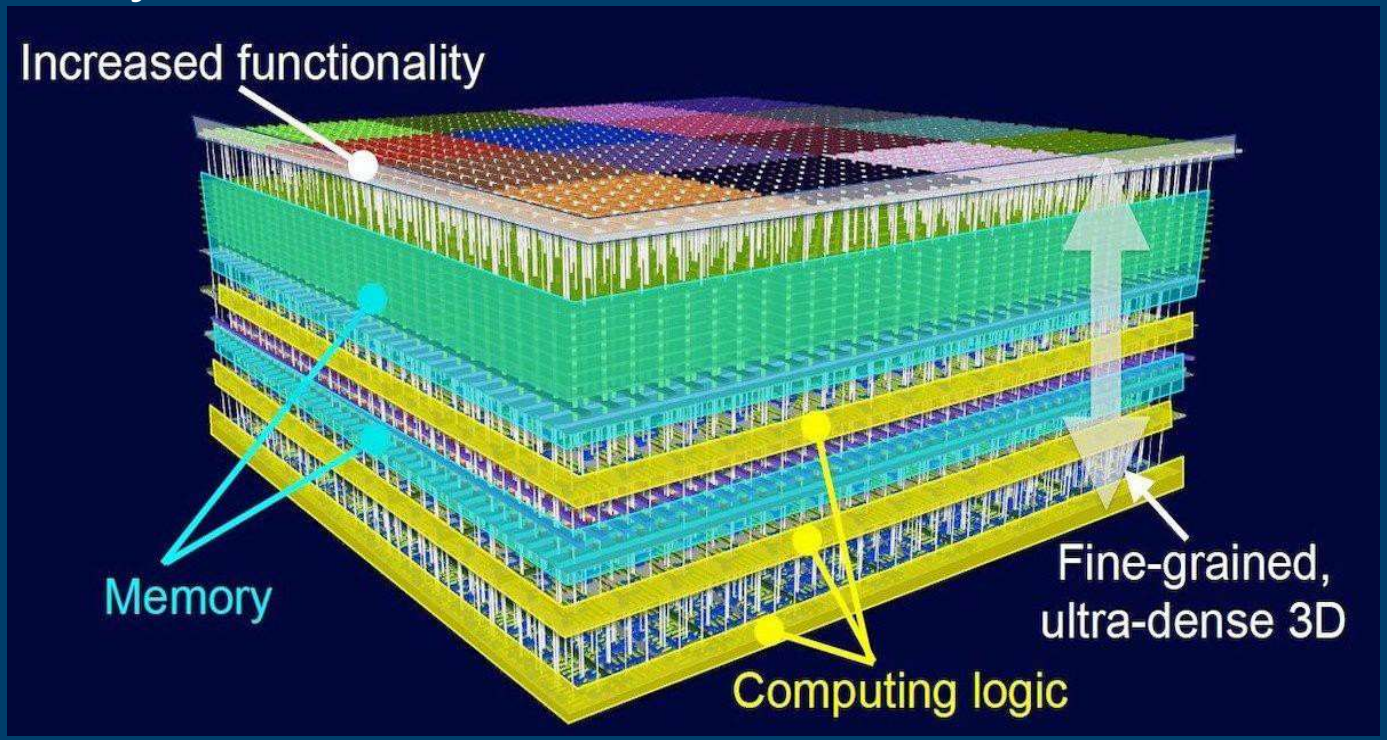


Soaring cost of chip design

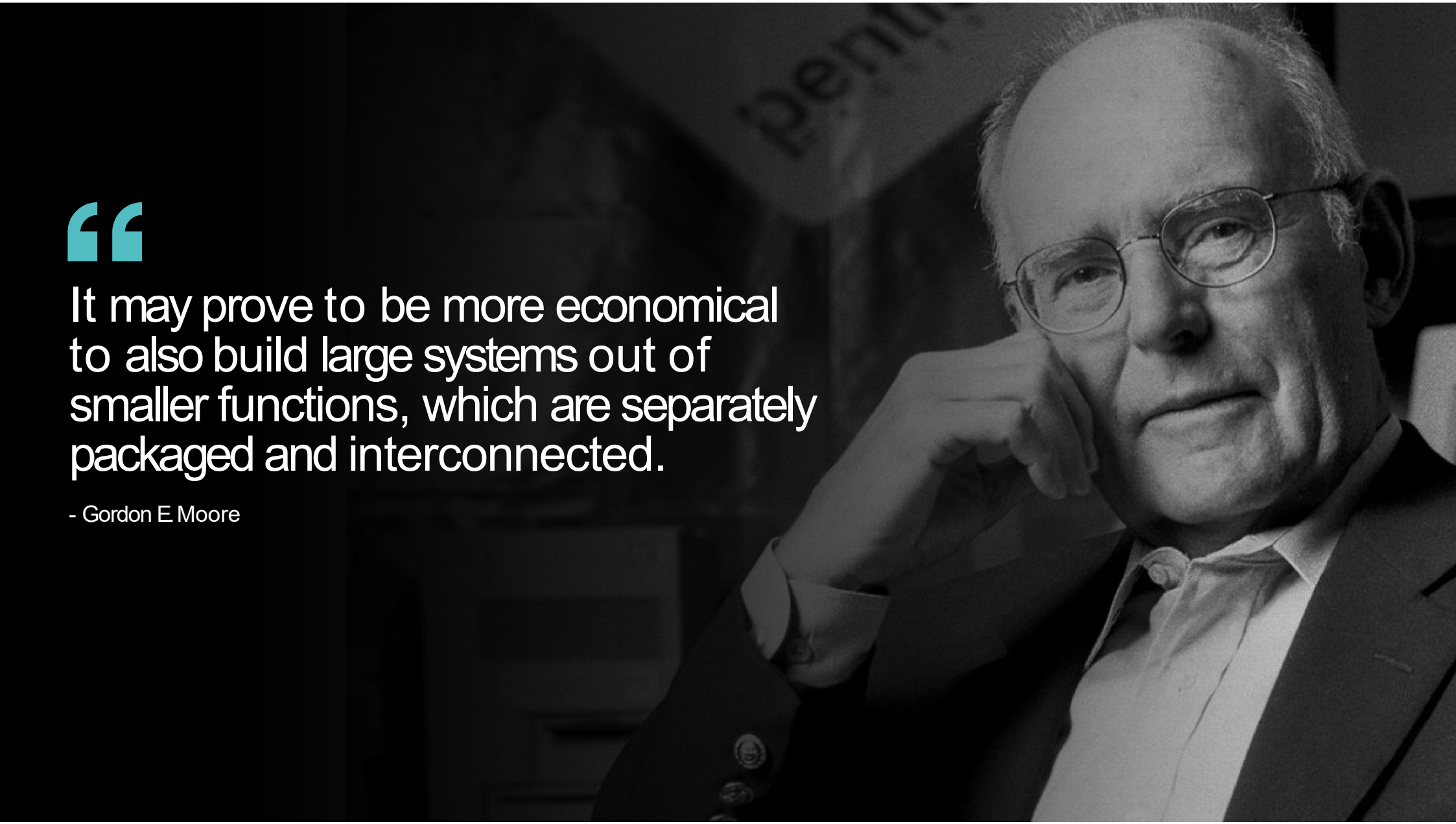


3D packaging - dramatically reduces wire lengths

- 95% of the power
- 98% of the delay



Source: NHANCED SEMICONDUCTORS 3DInCities


“
It may prove to be more economical to also build large systems out of smaller functions, which are separately packaged and interconnected.
- Gordon E Moore

Bob Patti Vision of the Future - Foundry 2.0

A new semiconductor industry paradigm is evolving…
A Finishing Foundry that takes the standardized building blocks from traditional semiconductor manufacturers and uses advanced packaging and additive manufacturing to create highly customized components with superior performance targeting small and medium sized markets.
(Essentially a semi fab without front-end-of-line)

Source: NHANCED SEMICONDUCTORS

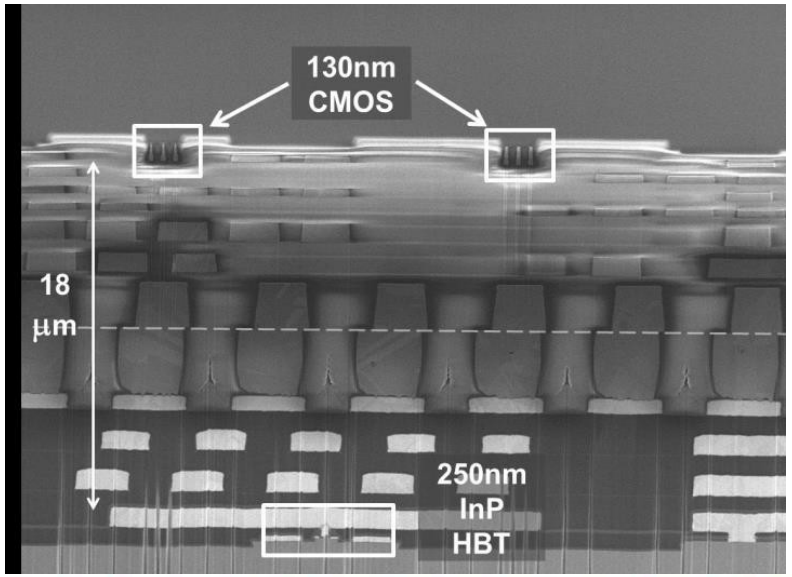
AP Elements: Bonding

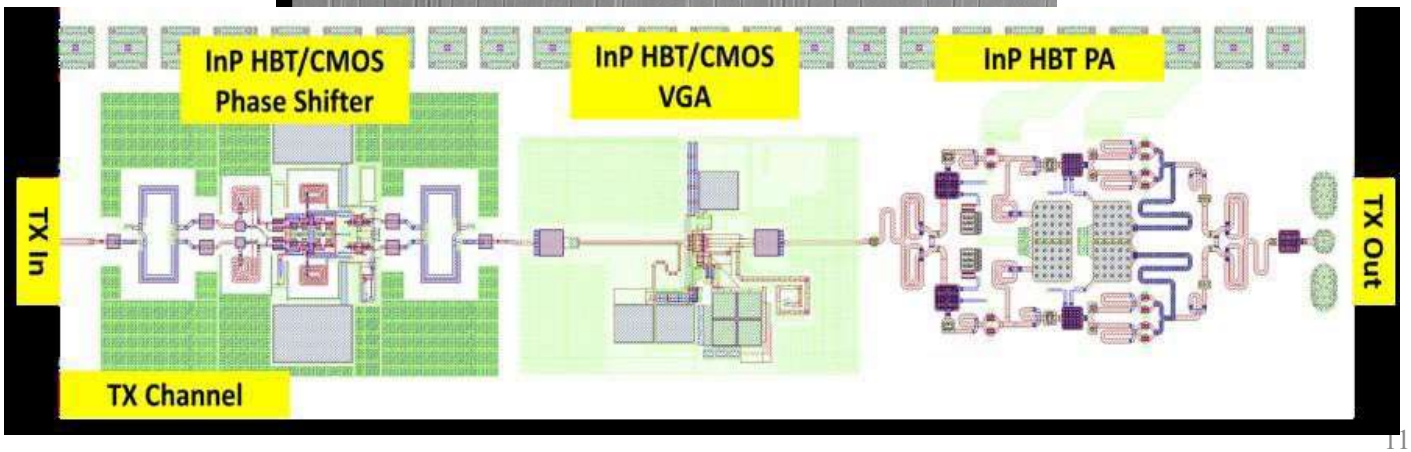
Millimeters ⇨ Microns

Kilograms ⇨ Grams

Mixed Materials

Best of Class



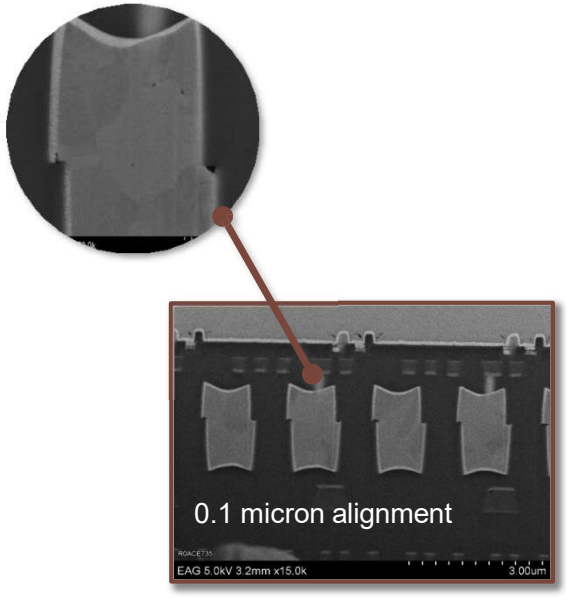


A Powerful New Tool: Hybrid Bonding – *One of Many*

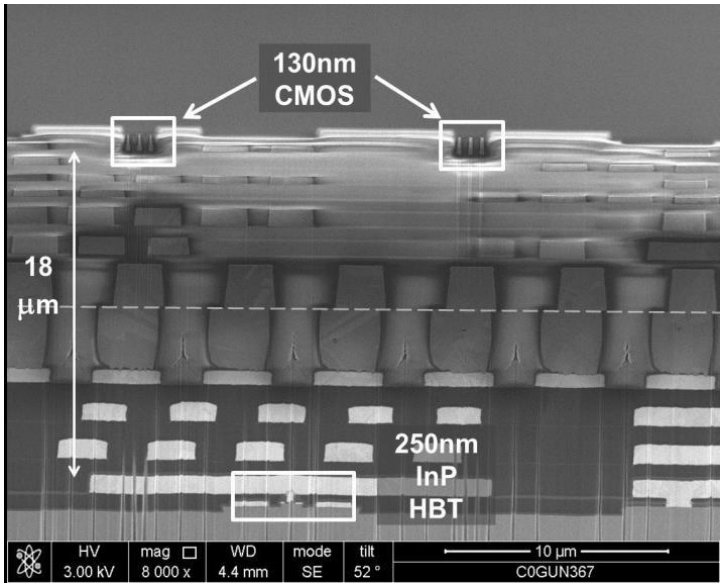
Millimeters ⇨ Microns

Kilograms ⇨ Grams

Mixed Materials ⇨ *Best of Class*



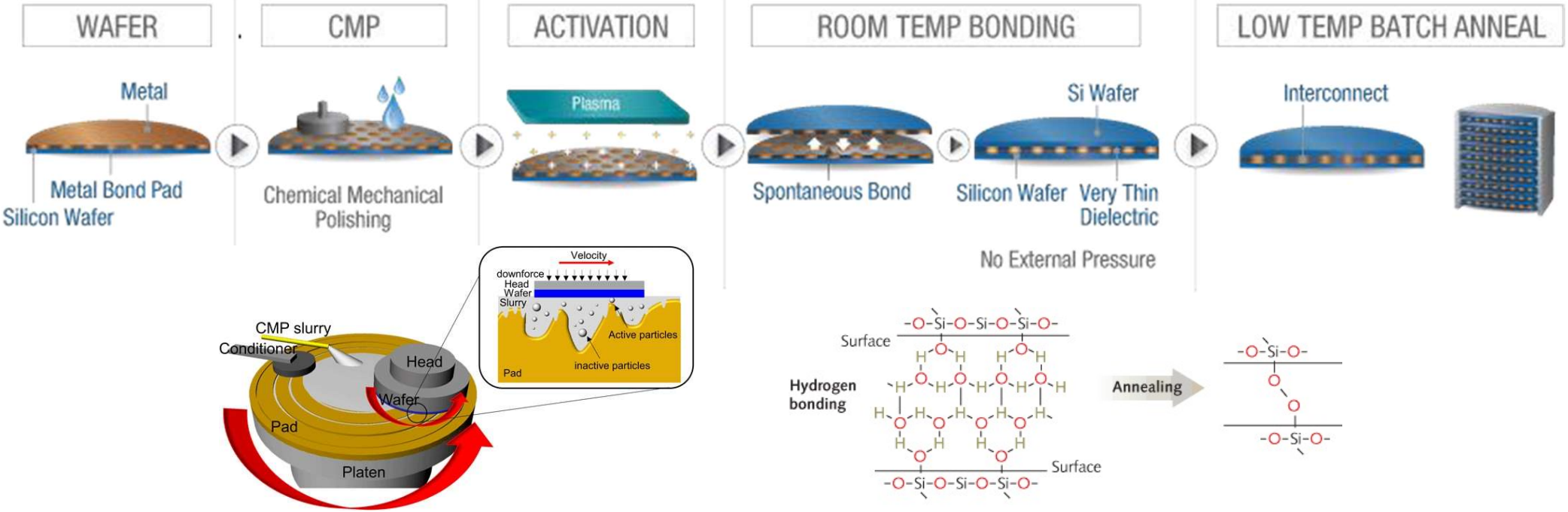
Global Foundries top wafer



Teledyne InP bottom wafer

NHANCED SEMICONDUCTORS

DBI®: Low Temperature Hybrid Bonding Process



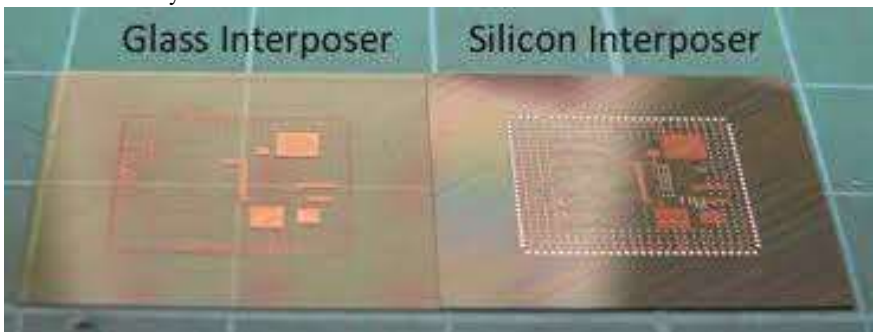
Jihoon Seo / Materials Research Society

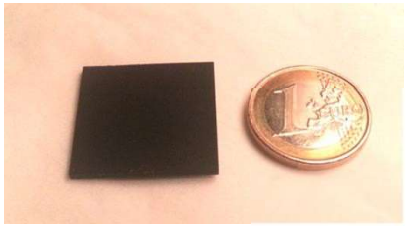
ENHANCED SEMICONDUCTORS

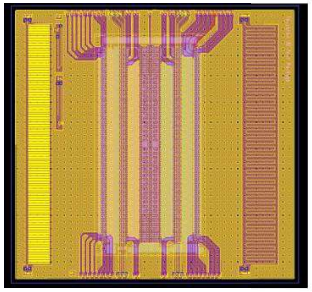
AP Elements: Interposers

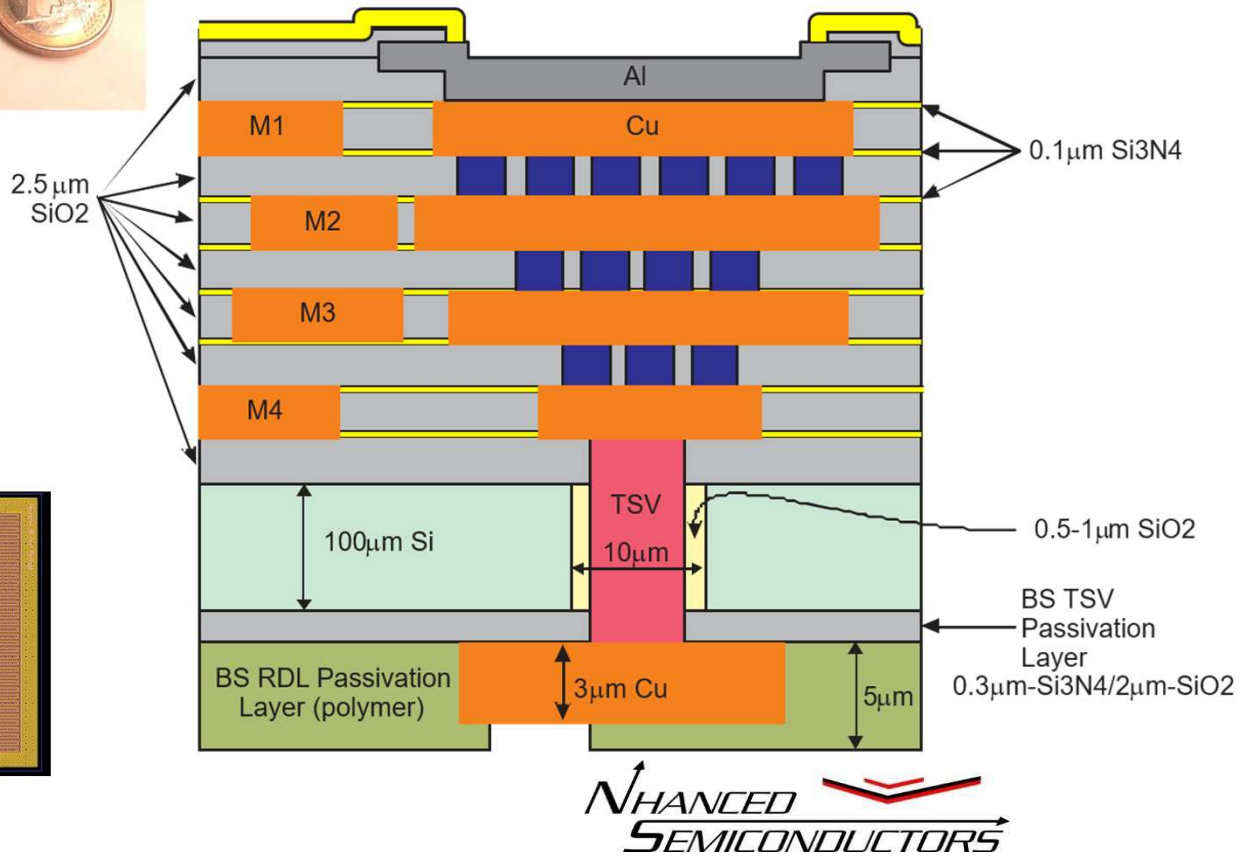
- Bigger, Better, Faster
- Lower Power

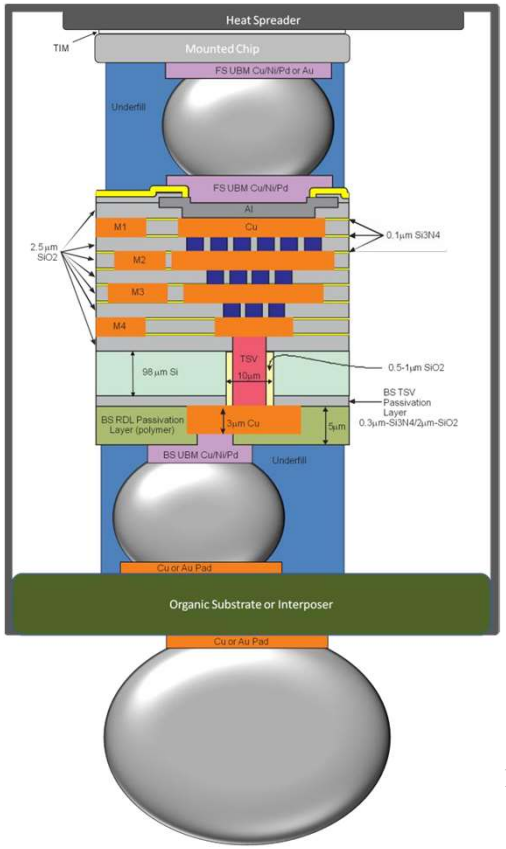
Mosaic Microsystems







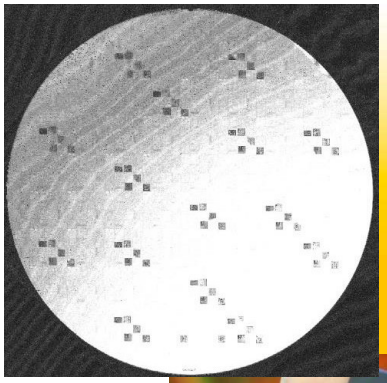


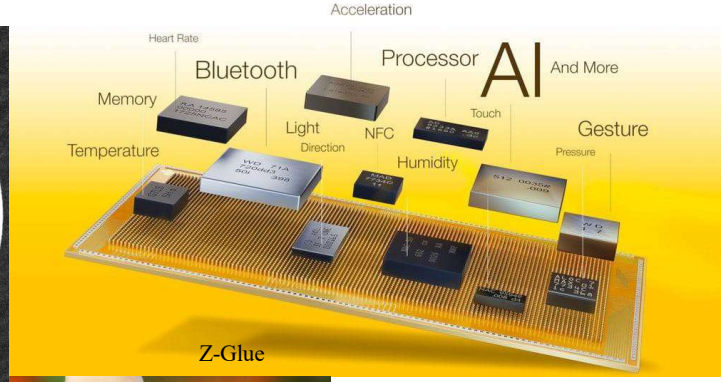


NHANCED SEMICONDUCTORS

AP Elements: Chiplets

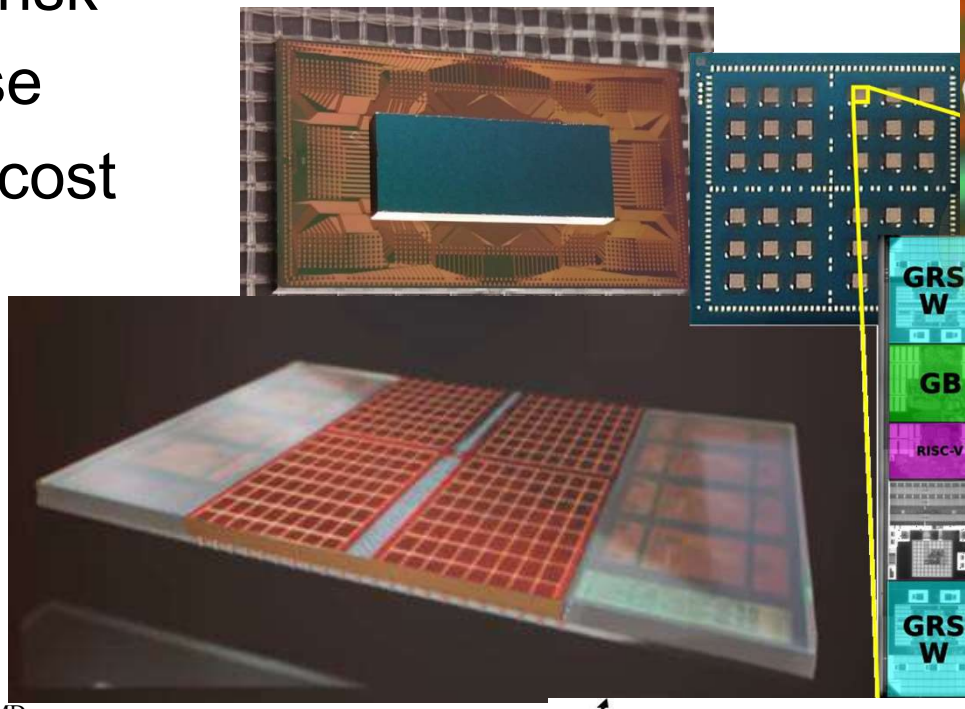
- Best of Class Everything
- Easy retargeting
- Lower risk
- IP reuse
- Lower cost

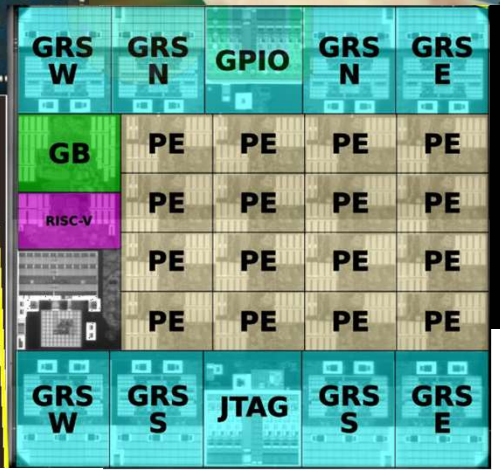




Z-Glue


Intel


AMD



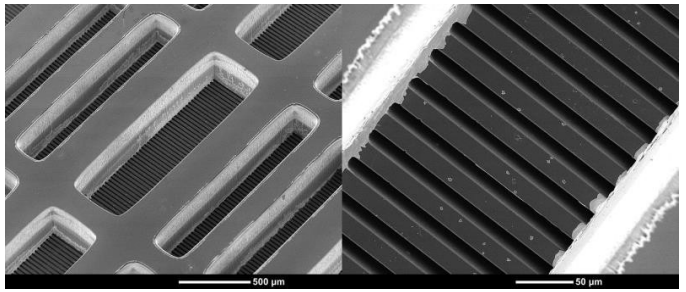
nVidia

Intel

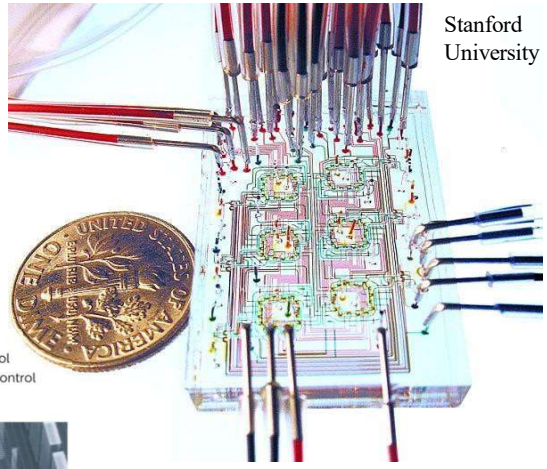
AP Elements: Microfluidics and Cooling

Chip Scale Cooling
For Ultra-Dense Electronics

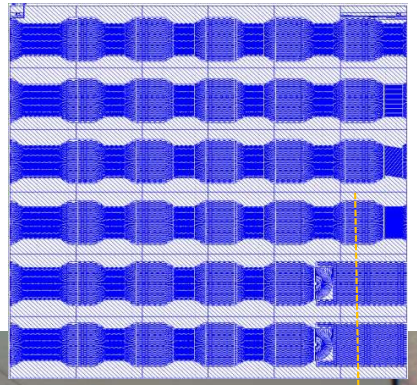
Purdue

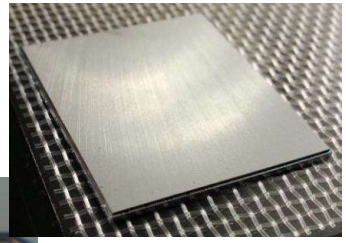


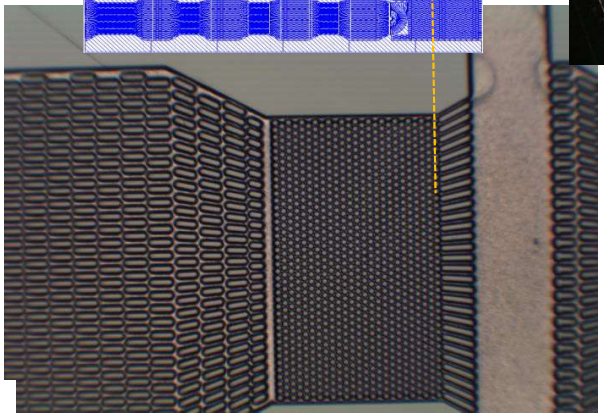
Biology + Electronics



Stanford University

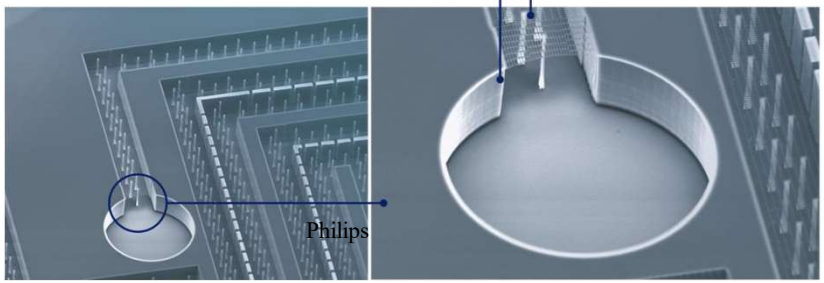






Our state-of-the-art tool set enables us to create microfluidic structures with accurate control:

- <5 degree slope control
- Sub-µm feature size control
- µm range feature size



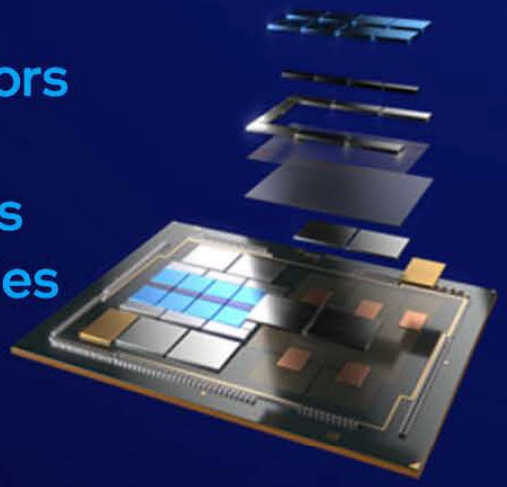
Philips

NHANCED SEMICONDUCTORS

Packaging advances to enable Integration of ever-increasing Functionality

Ponte Vecchio, HPC

>100B Transistors
5 Nodes
EMIB & Foveros
47 functional tiles



Industry Record for Integration

Blurring the boundary between wafer & package

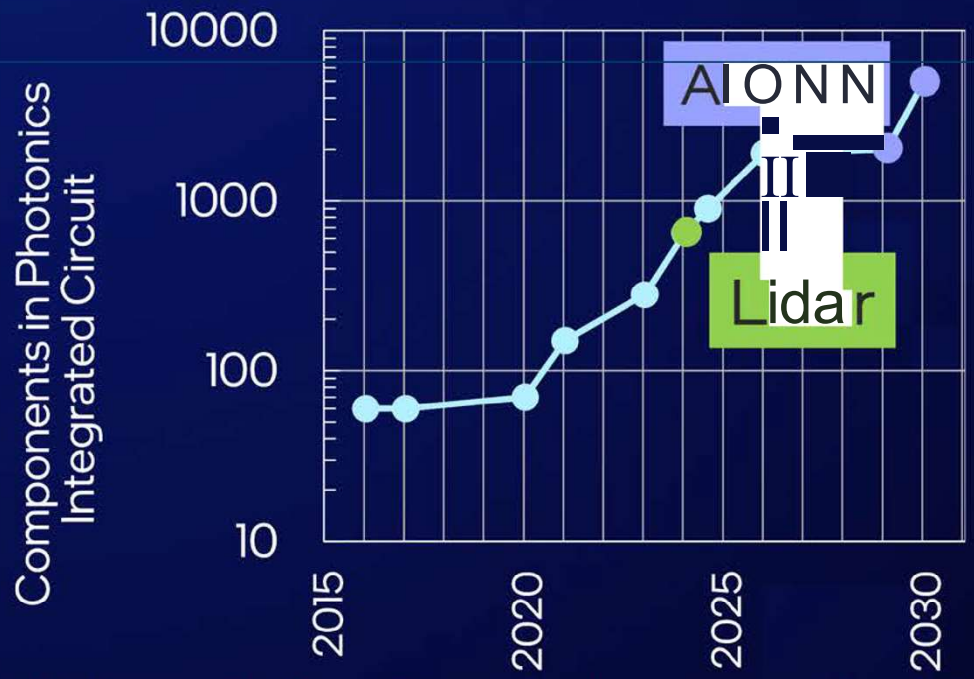
Industry leading Thermal-Power-Performance Modeling from Transistor to System

Integration of Silicon Photonics improves Reliability

Customer Data

>7M units shipped

Innovation in Silicon Photonics Integration

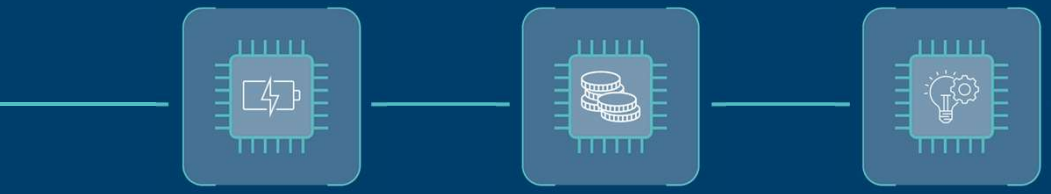


Rich portfolio of ready-to-use optical IP

A. Kelleher, IRPS 2023 keynote

The need for a more aggressive semiconductor & compute systems roadmap

1,000x
improvement / 5 years



How will we realize this exponential increase?

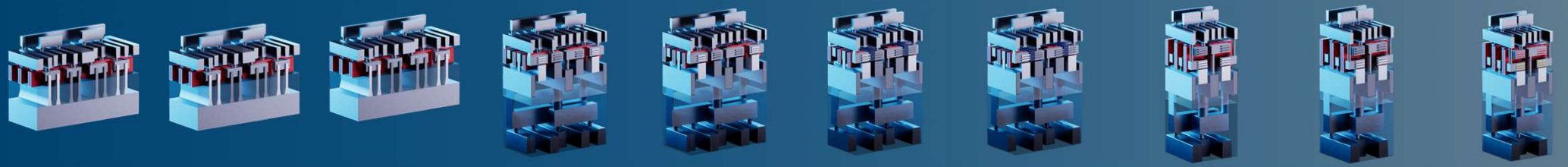
3D stacking provides linear complexity increase

3D stacking provides linear complexity increase

2D scaling provides exponential complexity increase

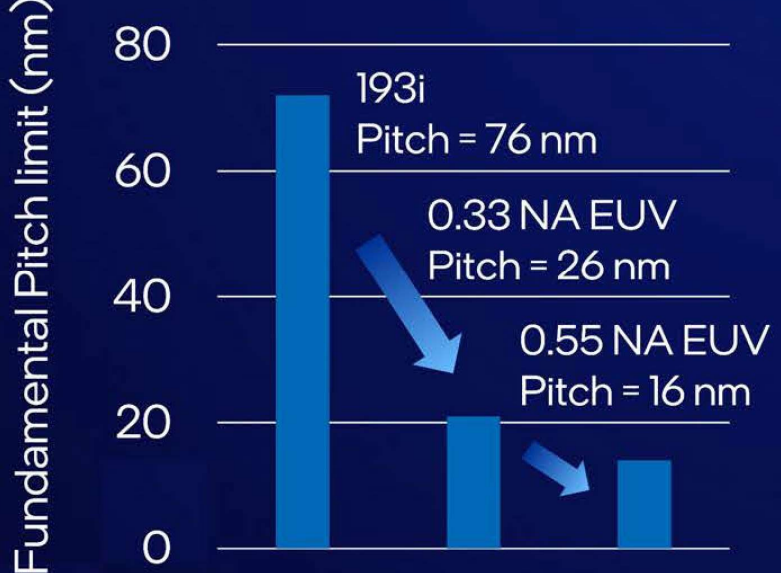
Potential roadmap extension

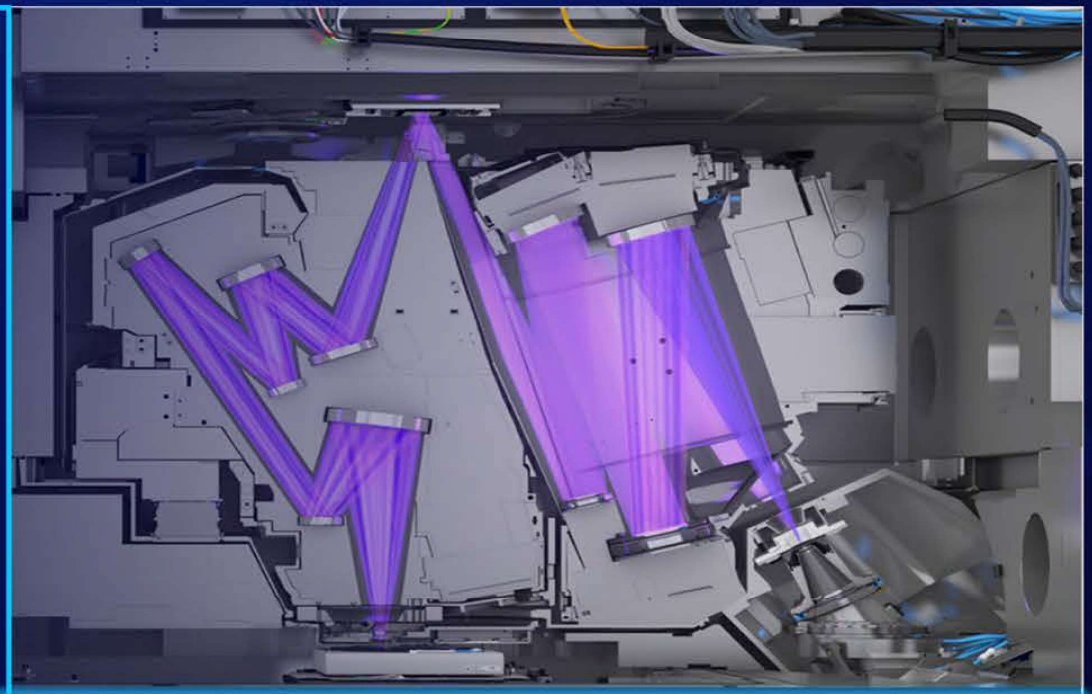
	N7	N5	N3	N2	A14	A10	A7	A5	A3	A2
Continued dimensional scaling										
Metal Pitch [nm]	40	28	22	21	18	16	16-14	16-12	16-12	16-12
Device and material innovations										
Metal Tracks	7	6	6	6	5	5	5	4	<4	<4
	FinFET	FinFET	FinFET	GAA Nanosheet	GAA Nanosheet	GAA Forksheet	GAA Forksheet	CFET	CFET	CFET Atomic
Context-aware interconnect										



Enabling high-NA EUV lithography

High-NA EUV improves resolution to enable further Silicon Technology Scaling

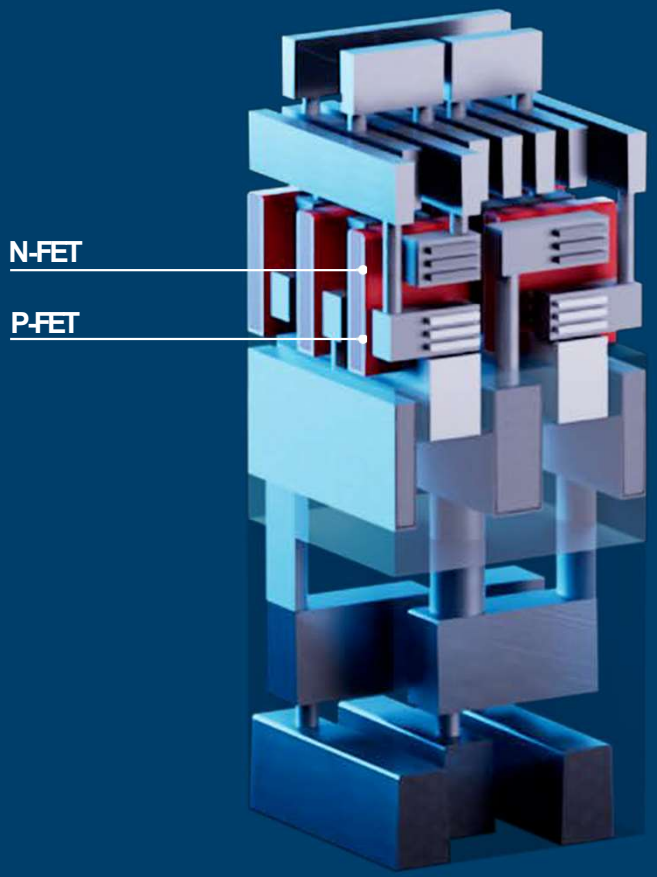




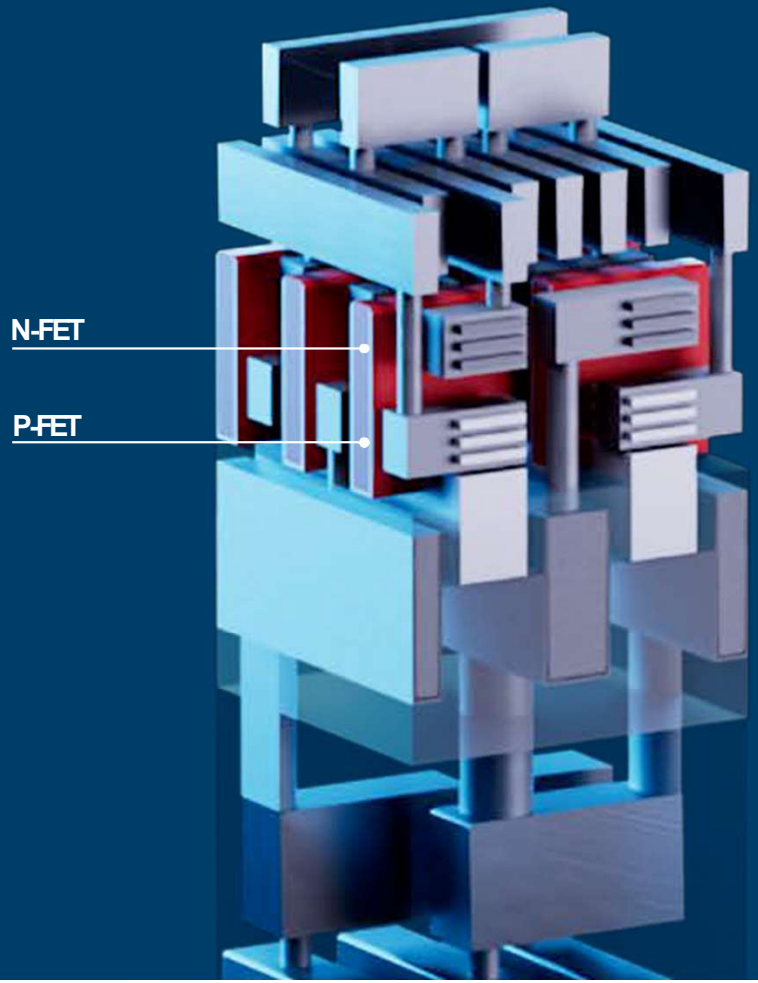
Intel in partnership with ASML will be the first to bring high-NA EUV to high volume manufacturing

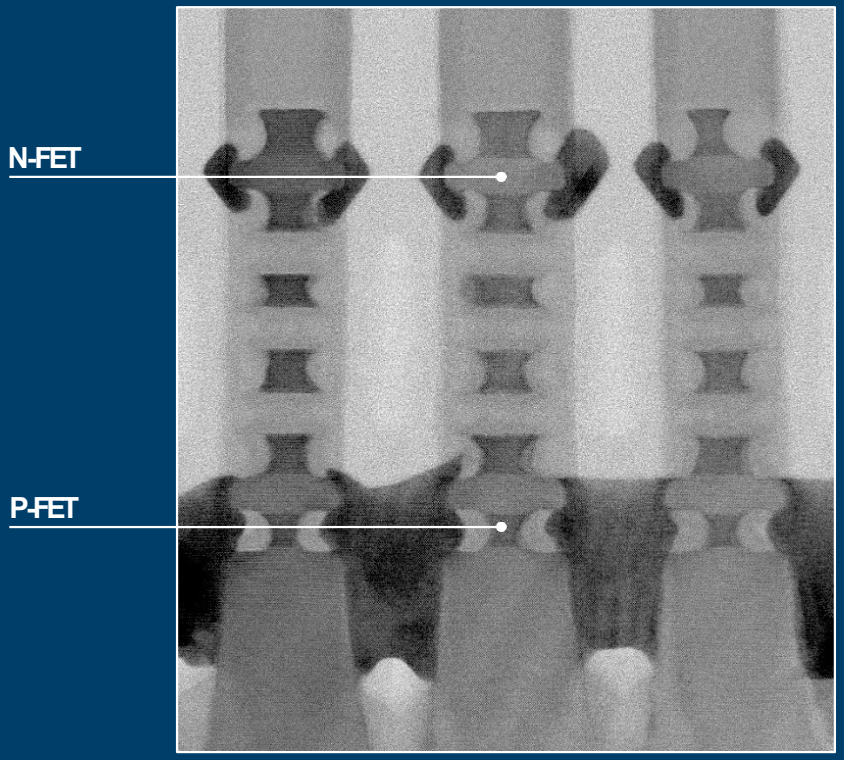
Image from ASML

Complementary FET (CFET)

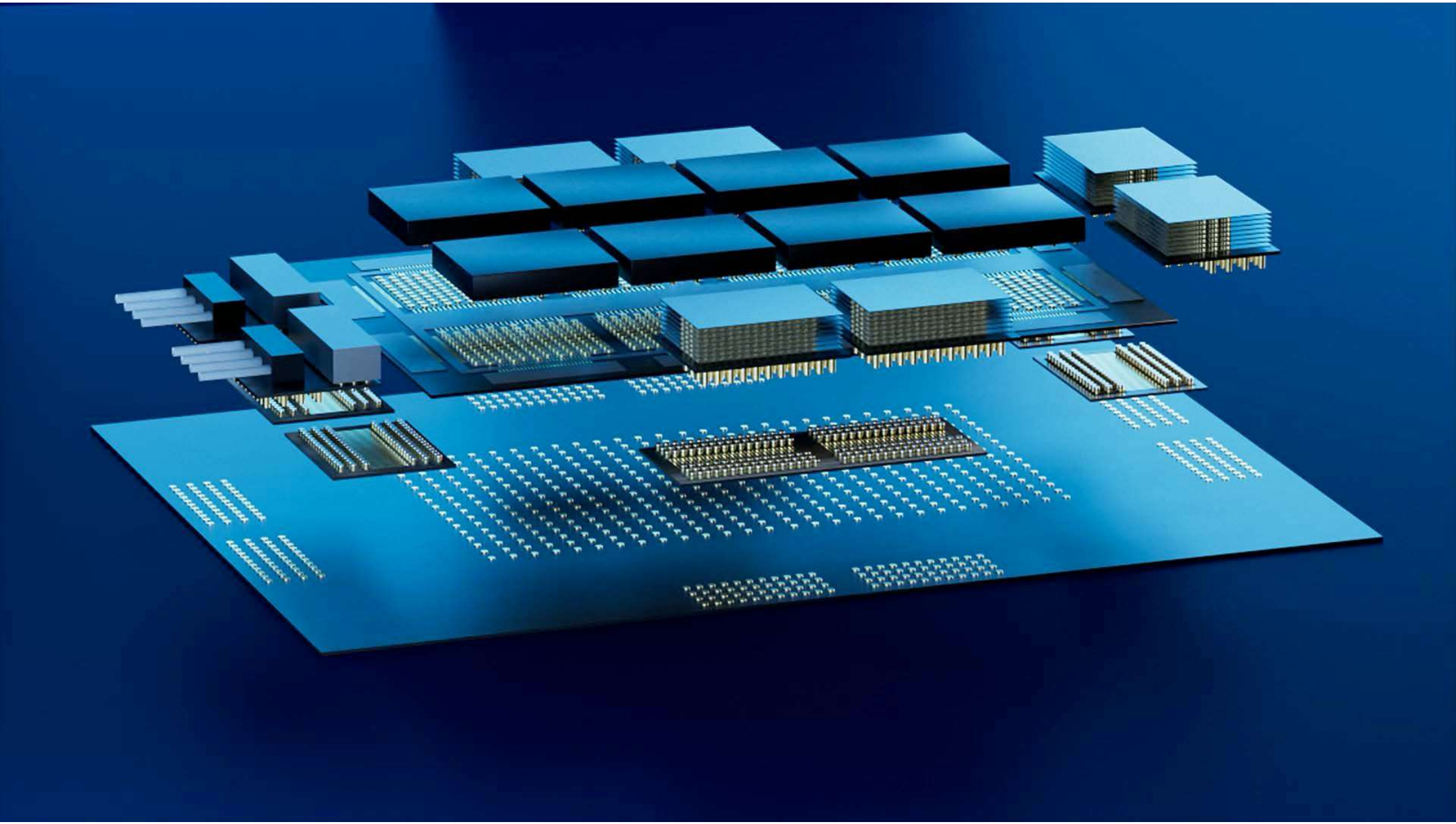


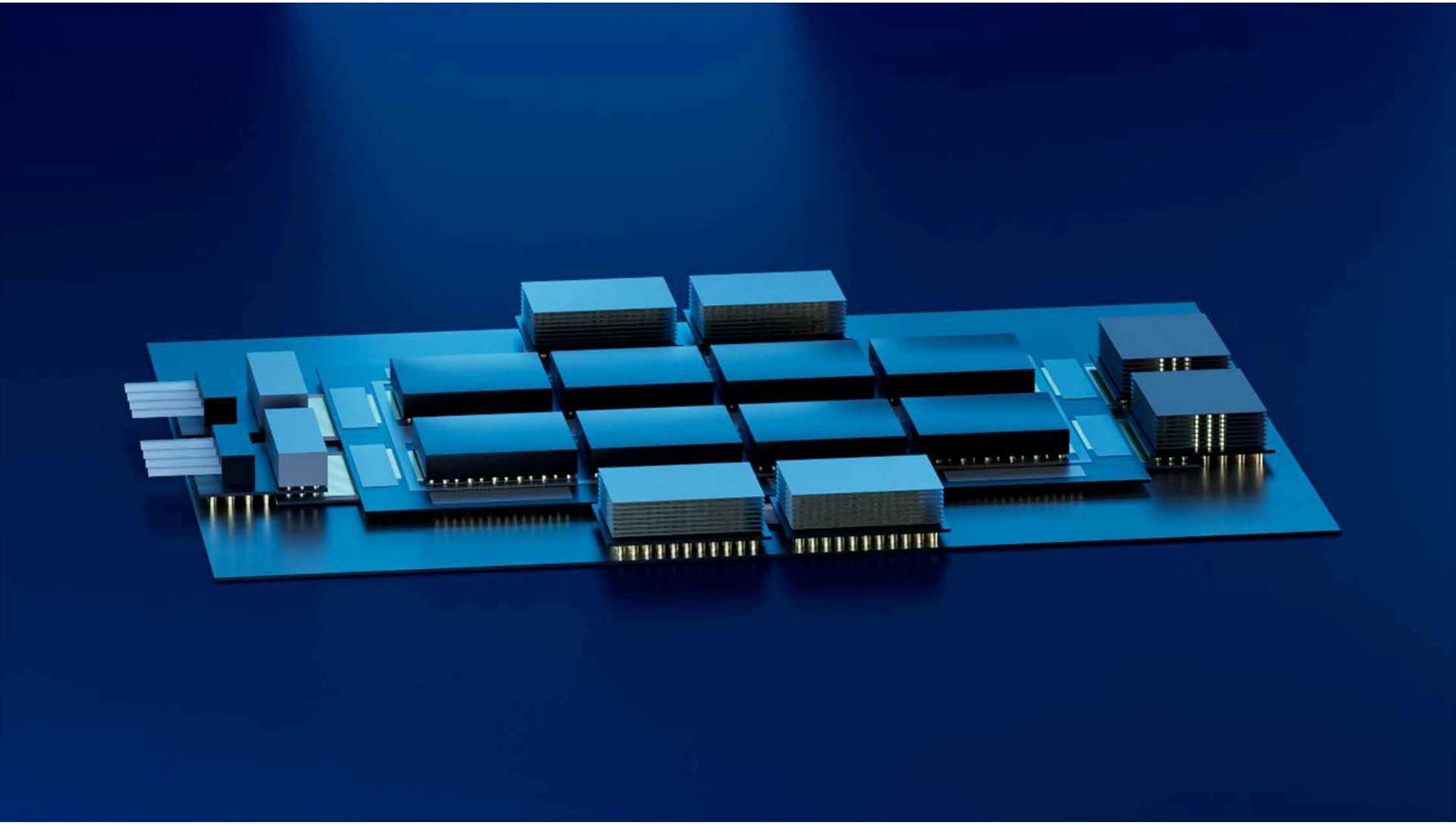
Complementary FET (CFET)

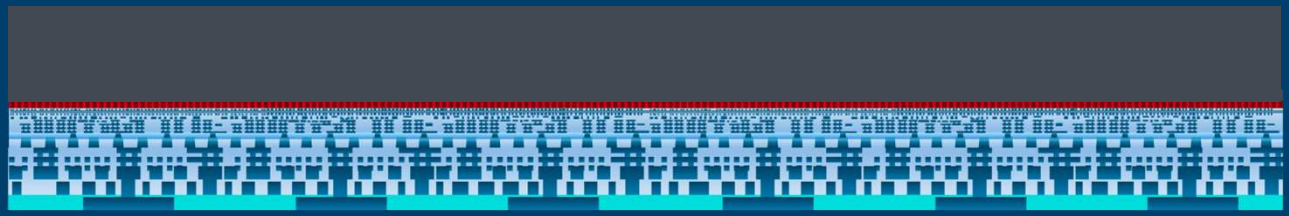




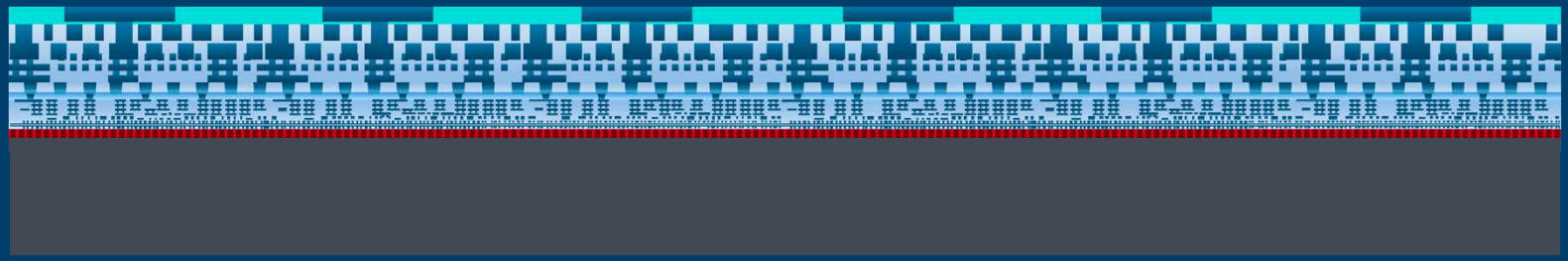
We need to combine a multitude of approaches



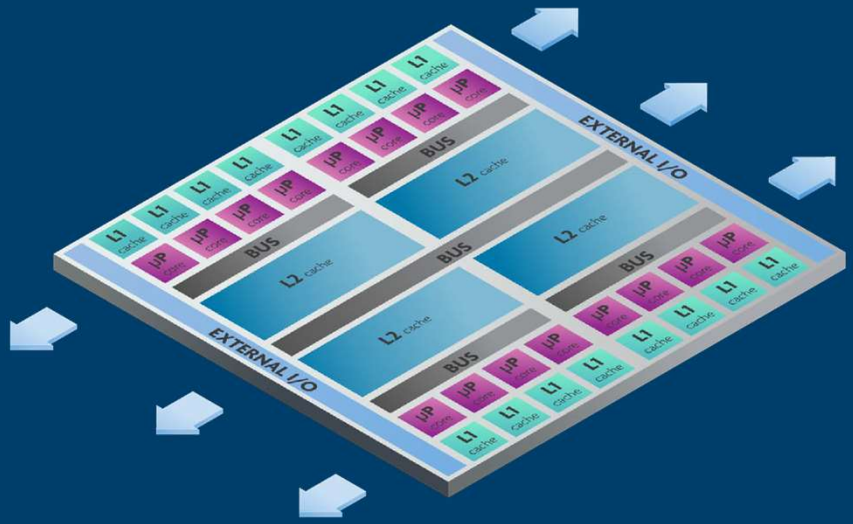




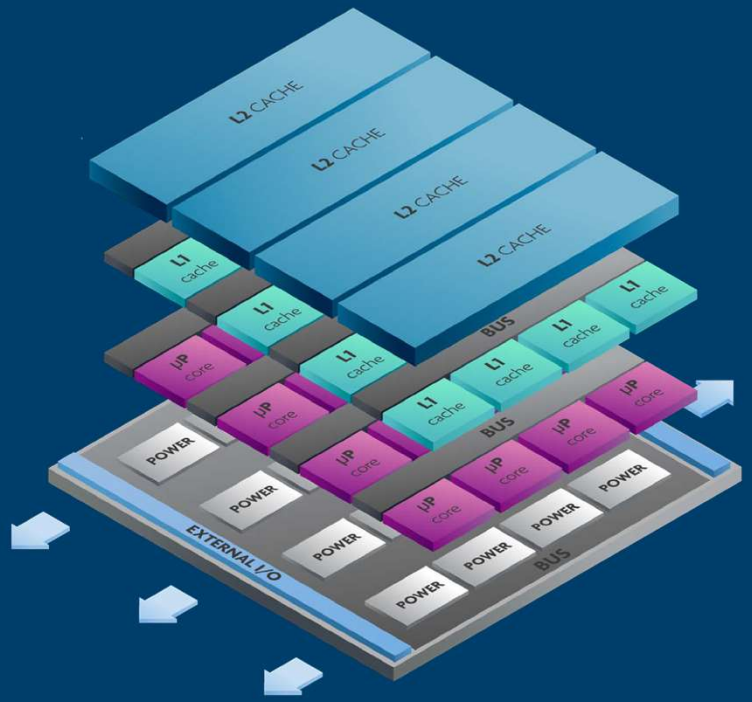
2D SoC

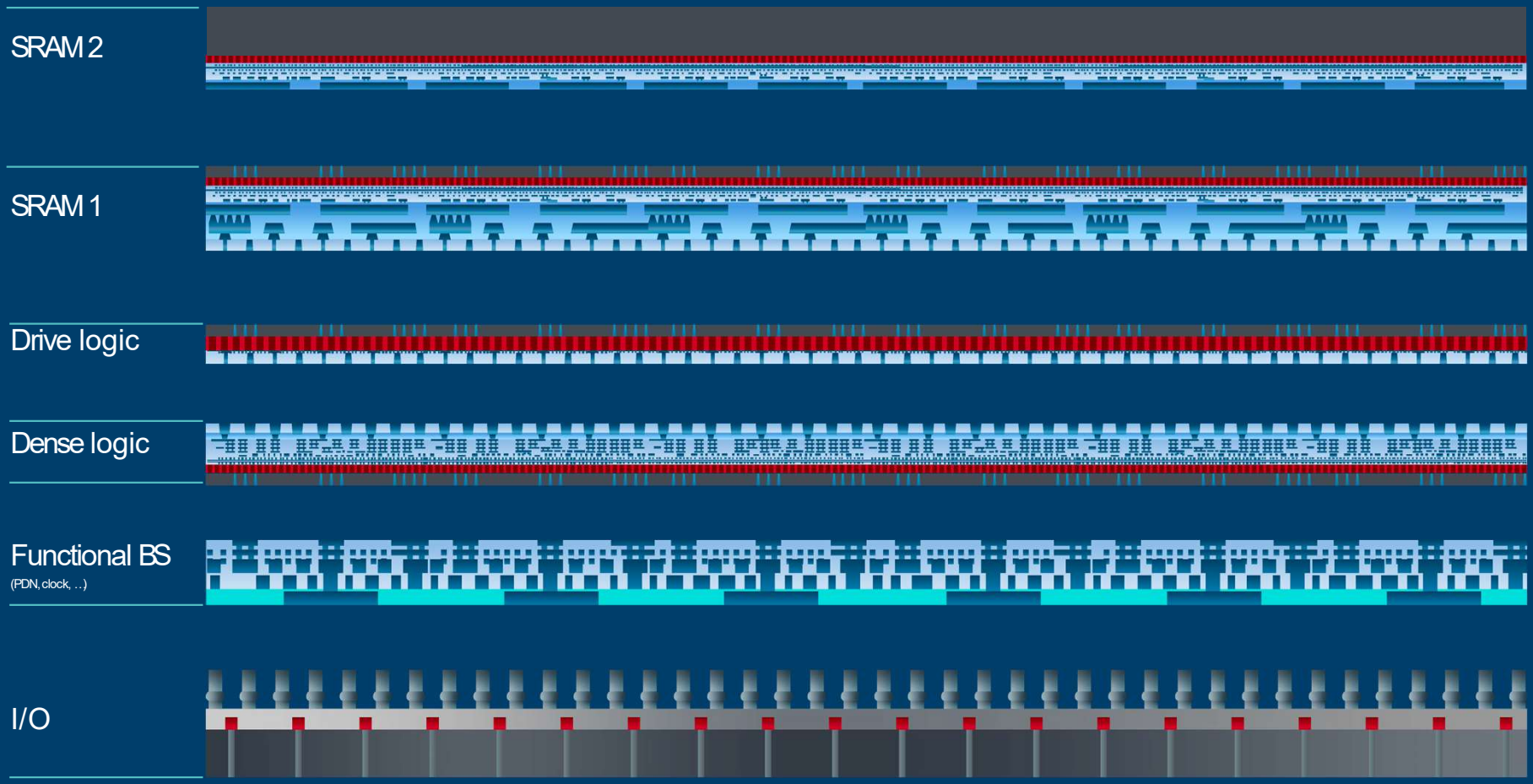


2D SoC


EXTERNAL I/O
EXTERNAL I/O
BUS
L2 cache
L1 cache
µP core

3D SoC


L2 CACHE
L2 CACHE
L2 CACHE
L2 CACHE
L1 cache
µP core
BUS
POWER
EXTERNAL I/O


SRAM 2
SRAM 1
Drive logic
Dense logic
Functional BS
(PDN, clock, …)
I/O

SRAM 2

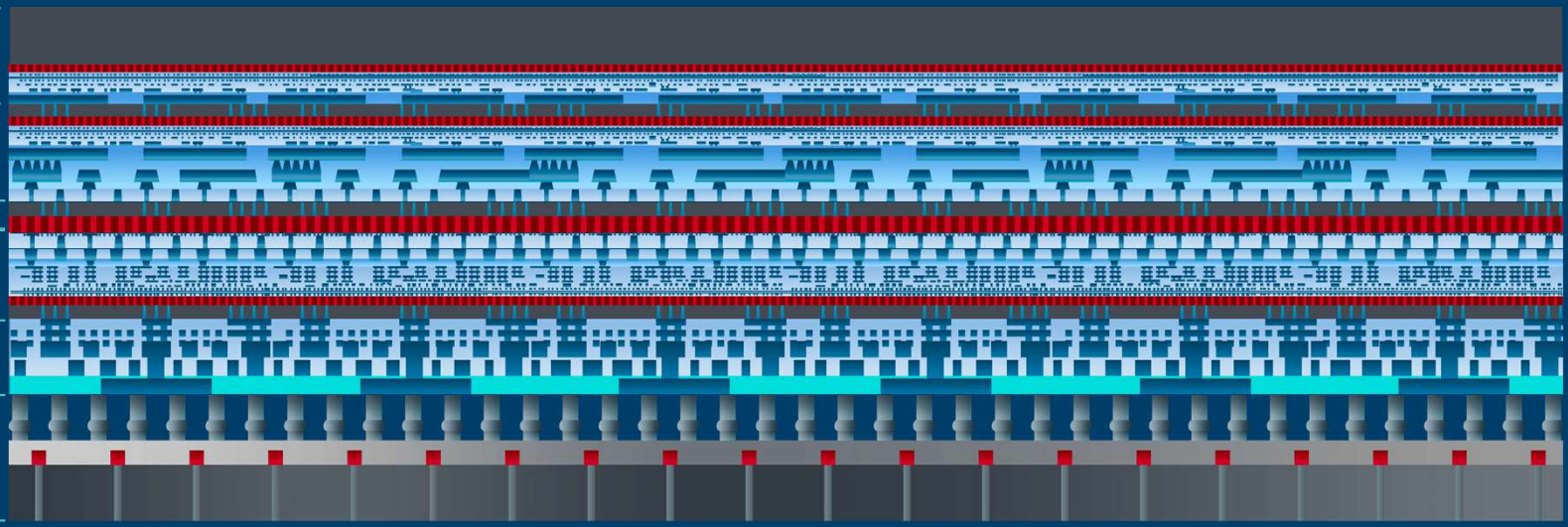
SRAM 1

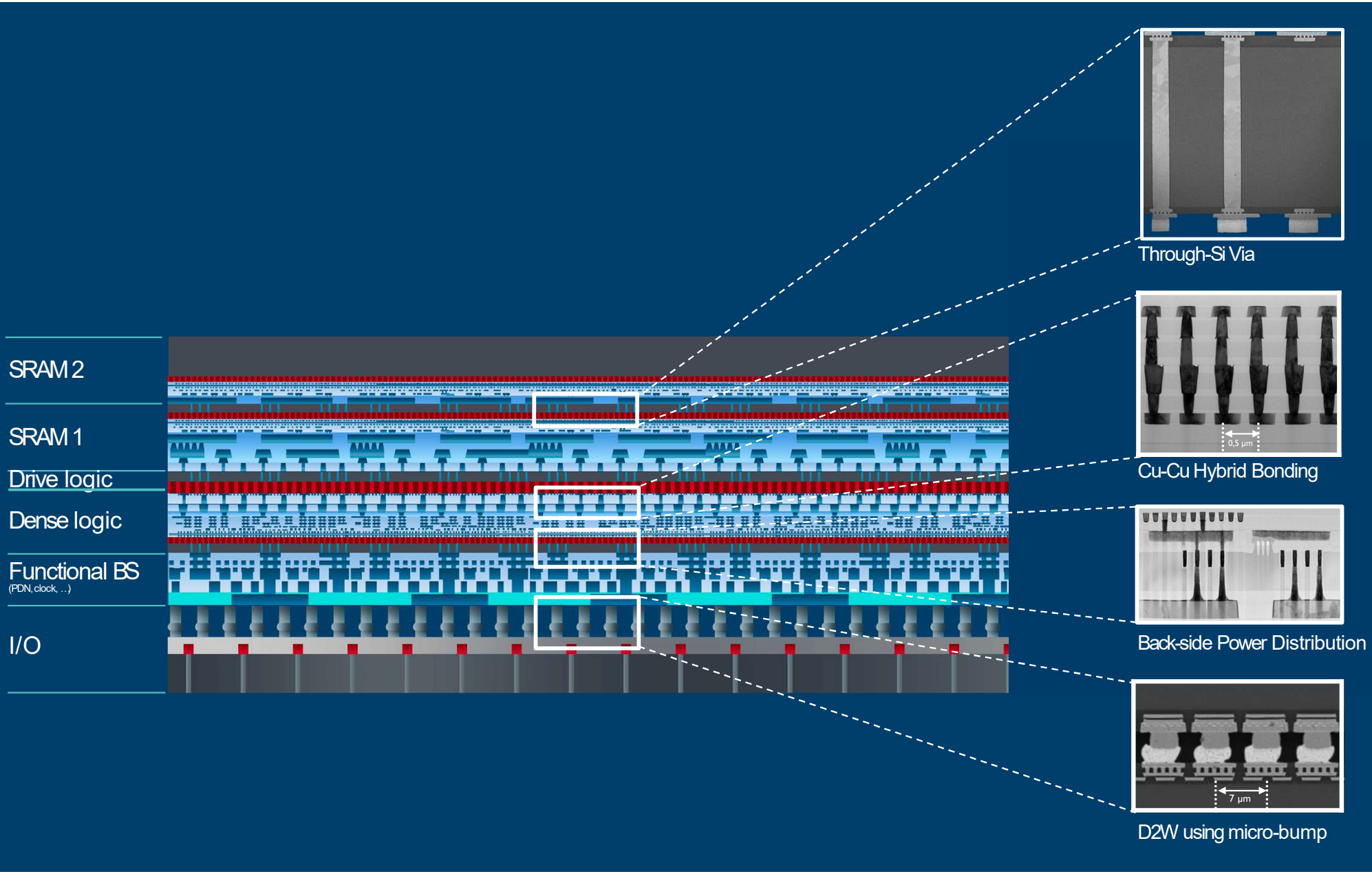
Drive logic

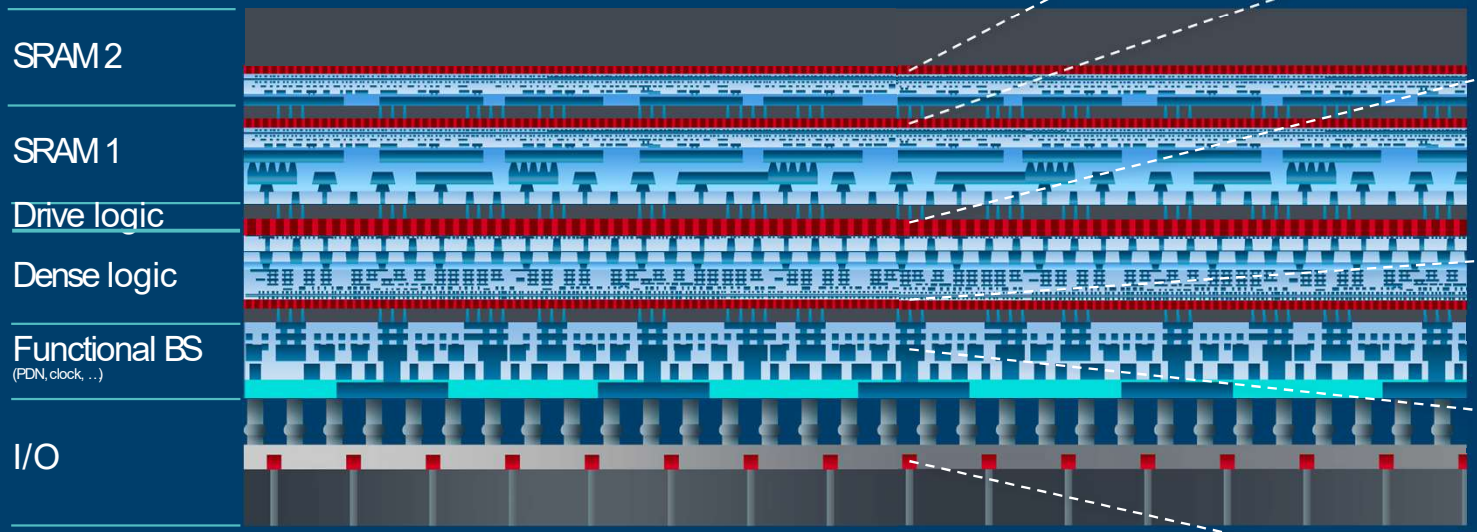
Dense logic

Functional BS
(PDN, clock, ..)

I/O




SRAM 2
SRAM 1
Drive logic
Dense logic
Functional BS
(PDN, clock, …)
I/O
Through-Si Via
0,5 µm
Cu-Cu Hybrid Bonding
Back-side Power Distribution
7 µm
D2W using micro-bump



FinFET - N5

FinFET - N3

Planar

CFET - A5

IGZO

Planar - N28-N14

Potential roadmap extension

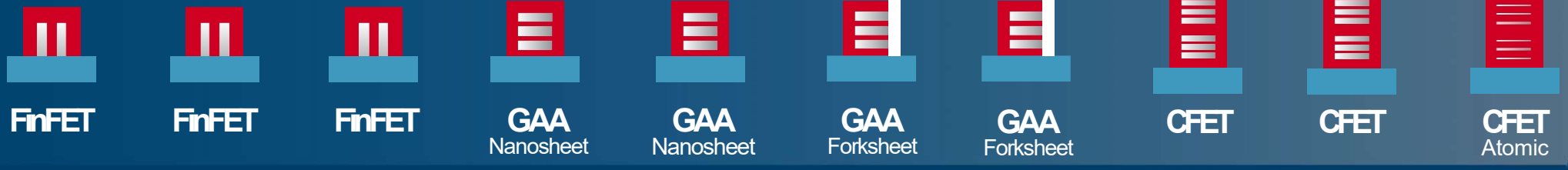
2018	2020	2022	2024	2026	2028	2030	2032	2034	2036
N7	N5	N3	N2	A14	A10	A7	A5	A3	A2

Continued dimensional scaling

Metal pitch [nm]	40	28	22	21	18	16	16-14	16-12	16-12	16-12

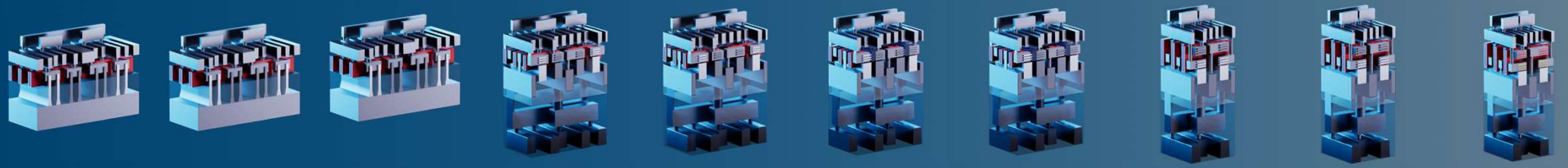
Device and material innovations

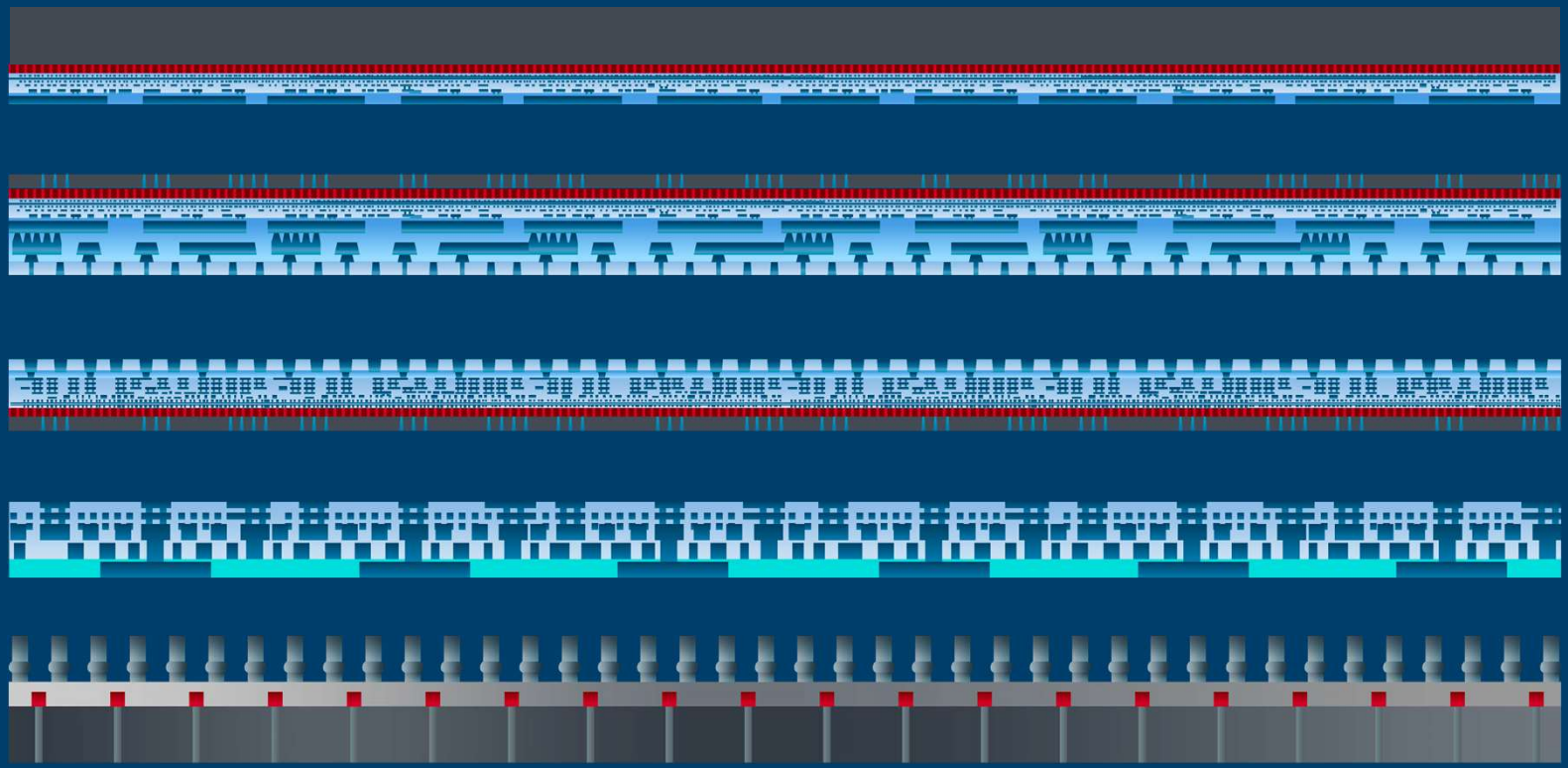
Metal tracks	7	6	6	6	5	5	5	4	<4	<4



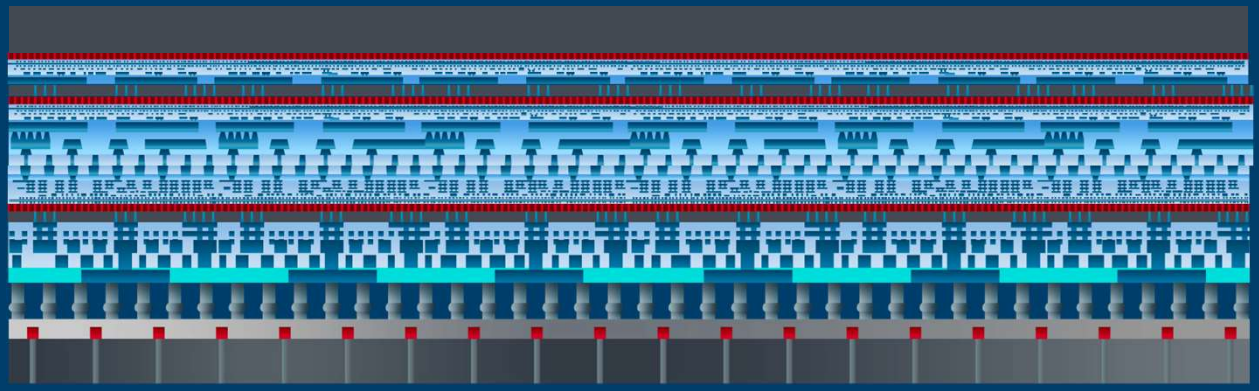
FinFET	FinFET	FinFET	GAA Nanosheet	GAA Nanosheet	GAA Forksheet	GAA Forksheet	CFET	CFET	CFET Atomic

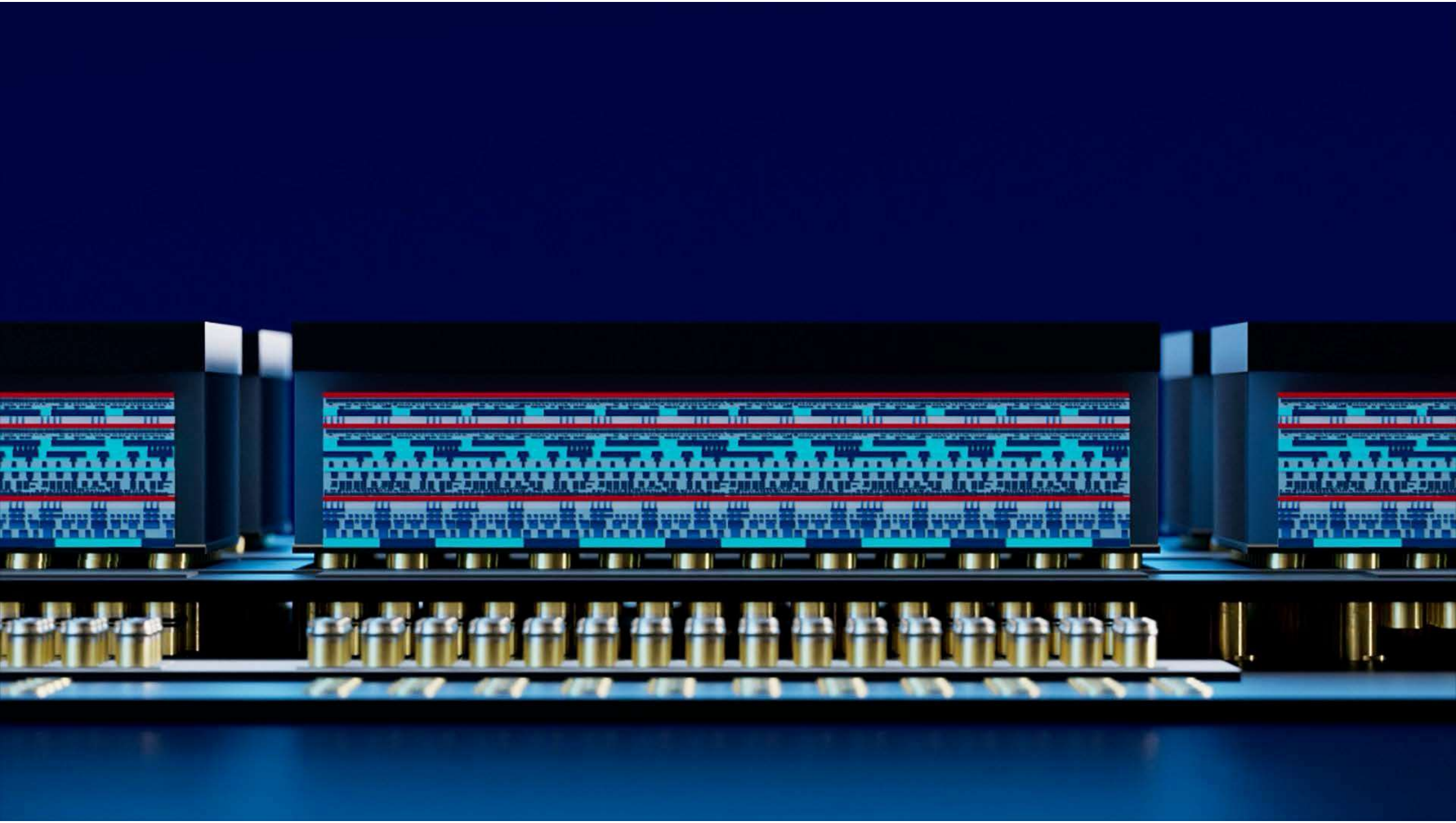
Context-aware interconnect





CMOS2.0





Thank You For Being Here!